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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,897	02/07/2001	Nobutaka Taniguchi	100353-00039	4758

7590 06/17/2005

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 600
Washington, DC 20036-5339

EXAMINER	
NGUYEN, LINH M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/777,897	TANIGUCHI, NOBUTAKA	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,4 and 6-8* is/are allowed.

6)☒ Claim(s) *1,2 and 5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

RCE acknowledgement/ Prosecution reopened

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after a final office action or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 05/18/2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant Admitted Prior Art (AAPA) (Figs. 1 and 3).

With respect to claim 1, AAPA, Figs. 1 and 3, discloses a delay time adjusting circuit with a corresponding method of adjusting a delay time of an input signal [Cin] so that a phase of the input signal and a phase of an output signal [Cout] match each other, the method comprises the steps of a) comparing [8] phases of the output signal and the input signal with each other, and b) increasing [10, 3] the delay time when a phase difference detected in the step of comparing indicates that the output signal is ahead of or behind the input signal.

With respect to claim 2, AAPA, Fig. 1, discloses that the method further comprises a step of producing the output signal by delaying the input signal by a DLL circuit [3].

With respect to claim 5, AAPA, Figs. 1 and 3, discloses a delay time adjusting circuit for adjusting a delay time of an input signal [Cin] so that a phase of the input signal and a phase of an output signal [Cout] match each other between phases based on a comparison of the input signal and the output signal, the circuit comprising a) detecting circuit [8] for detecting a phase difference between the phase of the input signal and the phase of the output signal; and b) delaying circuit [3] for increasing a delay time of the phase of the output signal when starting the delay time adjustment so that the delay time is set to a value at which the phase difference becomes N periods, where N is an integer other than zero.

Allowable Subject Matter

4. Claims 3-4 and 6-8 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

a) A delay time adjusting method including a step of adjusting a delay time of the input first periodic signal so that a phase of the input first periodic signal and a phase of the output second periodic signal match within a predetermined tolerance, in combination with the remaining claimed limitations, as called for in claim 3;

b) A delay time adjusting method including a second step of increasing the delay time to adjust a phase of an output second periodic signal so that, when the phase of a predetermined rising edge is judged to be behind the phase of the first rising edge in the first step, the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, in combination with the remaining claimed limitations, as called for in claim 4;

c) A delay time adjusting circuit for adjusting a delay time of an input periodic signal including a delaying circuit for adjusting said delay time so that, when the phase of a predetermined rising edge of an output second periodic signal is judged to be behind the phase of the predetermined rising edge of the input first periodic signal by a judging means, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, in combination with the remaining claimed limitations, as called for in claim 6; and

d) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal including an adjusting circuit for controlling a delaying circuit so that, when the phase of a predetermined rising edge is judged to be behind the phase of a first rising edge by a phase-detecting circuit, the delaying circuit delays the phase of an output second periodic signal until the phase of the predetermined rising edge and a phase of a second rising edge of an input first periodic signal match each other, the second rising edge being one period behind the first rising edge, in combination with the remaining claimed limitations, as called for in claim 7.

Remarks

6. Applicant's arguments filed 05/18/2005 have been fully considered but they are not persuasive.

With respect to the Applicant's argument regarding claim 1, at page 8, fourth paragraph, the examiner disagrees with the Applicant's statement "*the AAPA fails to disclose the feature of increasing [10, 3] the delay time when a phase difference detected in the step of comparing indicates that the output signal is ahead of or behind the input signal*". As clearly shown in the

AAPA, Fig. 1, when a phase difference is detected by the phase comparator [8] indicating that the output signal is ahead of or behind the input signal the delay adjuster [10] initiates an adjustment in the delay time [3].

With respect to the Applicant's argument regarding claim 5, at page 8, fourth paragraph, the examiner disagrees with the Applicant's statement *"AAPA does not show that the delay time is set to a value at which the phase difference becomes N periods."*. The delay time of the adjustment could be at any given number of periods in order to produce the matching and locking of the phases of the delay clock signal [dclk] and the target clock signal [tclk], which encompasses N periods when the detected phase difference is N periods.

Moreover, still with respect to the Applicant's argument regarding claim 5, at page 9, first paragraph. The Applicant stated "*dclk is in synchronization with tclk with a delay of one period, ... That is, N is equal to 1 (N=1)... Thus N=0 never happens in AAPA*"; the Examiner is not quite clear on what this argument is all about, as understood, the Applicant basically confirms that AAPA does disclose the claimed limitation "*where N is an integer other than zero*" (last line of claim 5).

Consequently, claims 1, 2 and 5 remain rejected as set forth in the office action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER